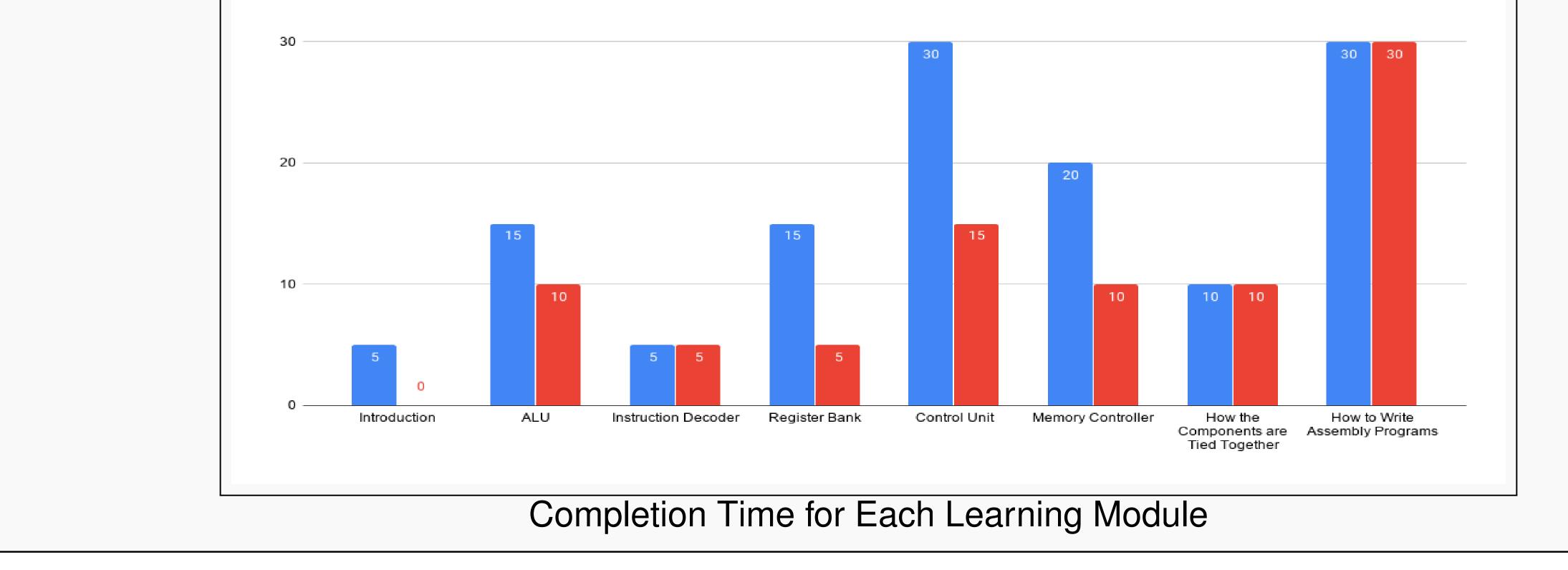
Baskin Engineering SANTA CRUZ Kai Tamkun, Rosario Jauregui, Rayne Jones, Tiffany Luong, Harvey Xu

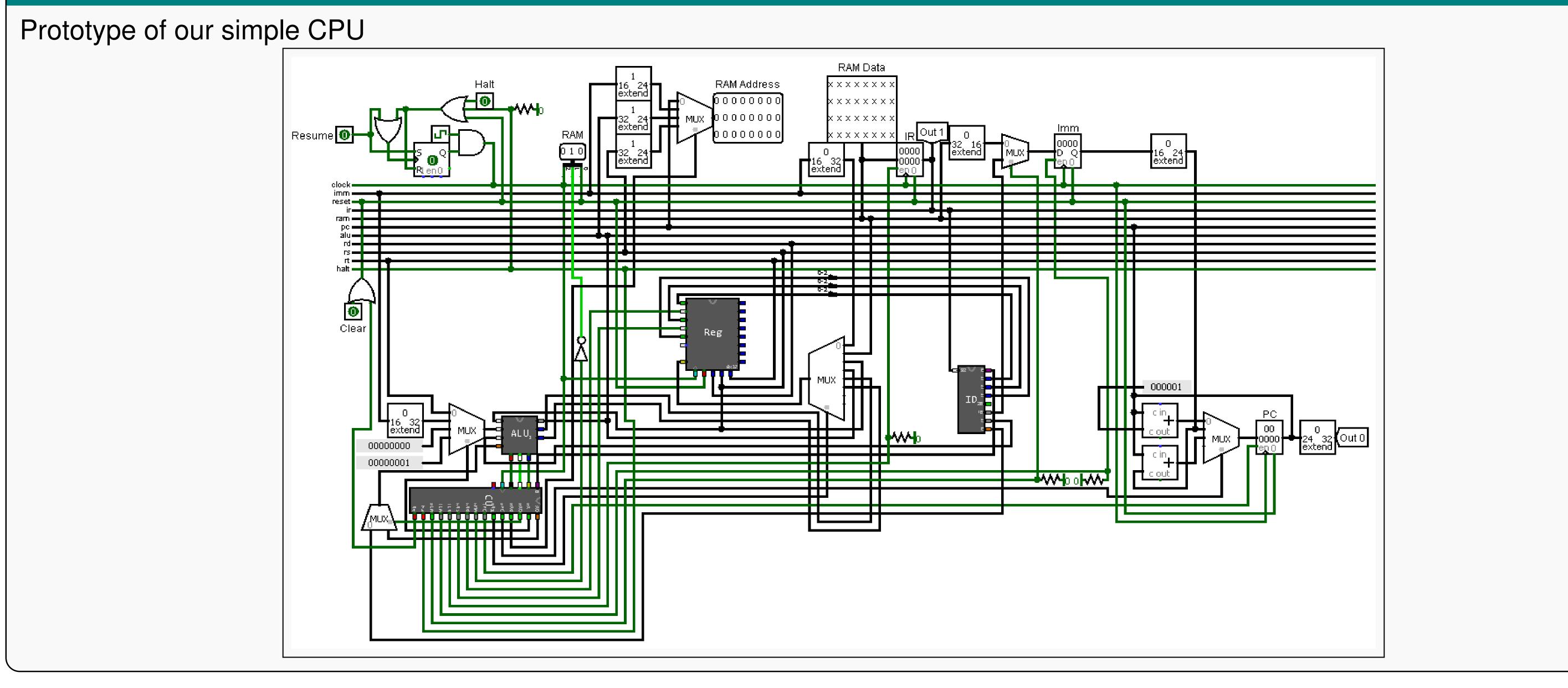
INTRODUCTION

Need: It's too hard for beginners to learn about CPU design
Goal: Make it easier for beginners to learn about CPU design
Design Objectives: Produce a complete CPU design that includes seven lessons and practice exercises at the end of every lesson
Target Audience: Educational institutions that want to use a simplified CPU to teach a class and self-learners
Learning Modules: The completion time of the entire lesson plan is 3.6 hours

Documentation Examples



CPU DESIGN



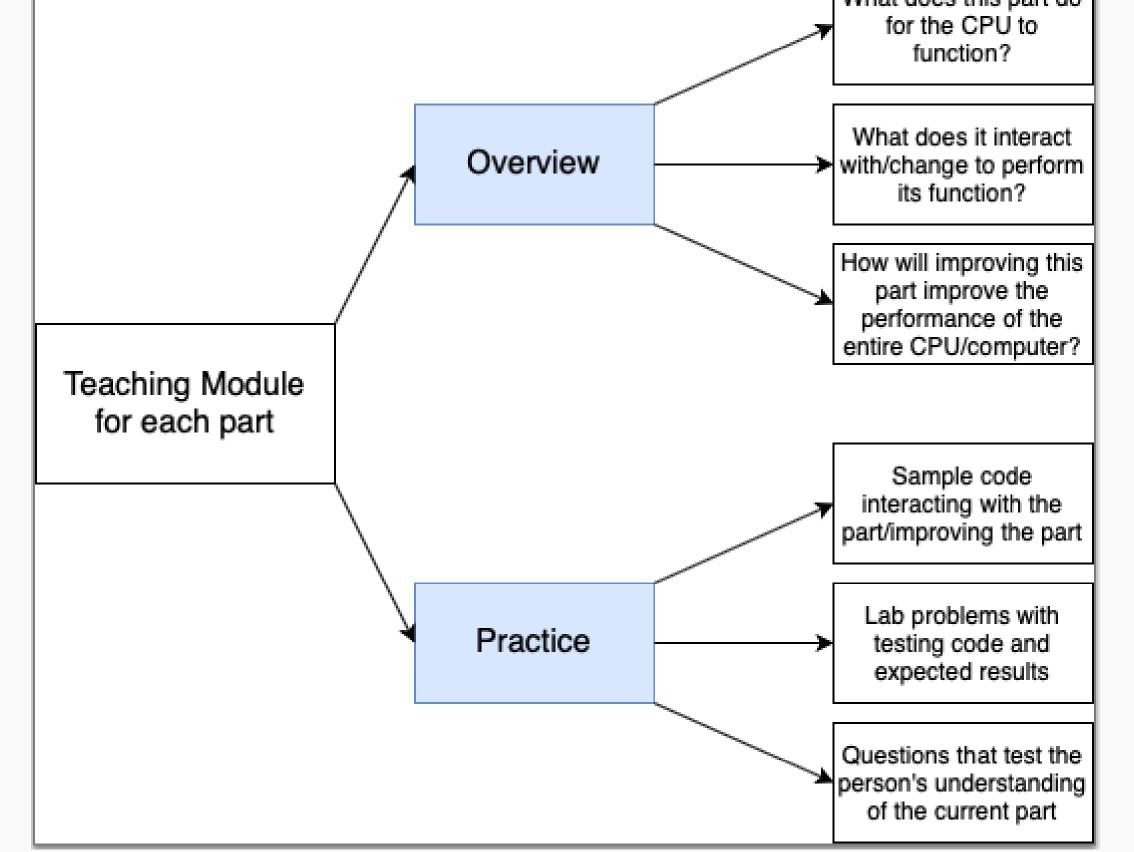
TEACHING STRATEGY

The types of questions each learning module aims to answer is shown below

What does this part do

ASSEMBLY CODE

Each line represents the machine code to the corresponding assembly code from a virtual machine



0x 01f000000000002	< <u>halt</u> >
0x 012001000000006	[\$rt
0x 012000c00000006	[\$fp
0x 012009c00000006	[\$t0
$0 \times 01200a000000006$	[\$t1
$0 \pm 01200a400000006$	[\$t2
$0 \times 01200a800000006$	[\$t3
0x 002040018000004	\$sp -> \$fp
0x 01e001660000008	\$sp % 8 -> \$m0
0x 001cc0810000001	\$sp -= \$m0
0x 002040138000004	\$sp -> \$t0
0x 004001020000008	\$sp -= 8
$0 \times 012005 d38000002$	\$a0 -> [\$t0]
$0 \times 012009 d4 00 00 01$	[\$t0] -> \$t1
0x 002500148000004	\$t1 -> \$t2
0x 003014aafffffe8	\$t2 + 4294967272 -> \$t3
0x 002060010000004	\$fp -> \$sp
$0 \times \ 00 \ 25 \ 40 \ 03 \ 80 \ 00 \ 00 \ 04$	\$t3 -> \$r0

ADMIN

Contact: tiluong@ucsc.edu Github: https://github.com/heimskr/educpu, https://github.com/heimskr/why.js